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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,459	03/01/2004	Eric Chen-Li Sheng	TRAN-P282	3462

7590 09/01/2004

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EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 09/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,459	SHENG ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: on page 1, line 5, after the words "Serial Number" insert --10/791,241--, on page 1, line 6, after the words "filed on" insert --March 1, 2004--, on page 1, line 11, after the words "Serial Number" insert --10/791,099--, on page 1, line 12, after the words "filed on" insert --March 1, 2004--.

Appropriate correction is required.

Claim Objections

2. Claim 4 is objected to because of the following informalities: in line 1 of claim 4, the limitation "a voltage supply" should be changed to --the voltage supply-- in order to limit a duplicant positive recitation in the claimed since claim 4 depends from claim 1.

Appropriate correction is required.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-22 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No. 10/791,241.

Regarding claims 1-22 of this application, claims 1 and 15 of this application correspond to claim 1 of U.S. Application 10/791,241, claims 2 and 16 of this application correspond to claim 2 of the other application stated above, claims 3 and 17 correspond to claim 3 of the other application, claims 4 and 18 correspond to claim 4, claims 5 and 19 correspond to claim 5, claims 6 and 20 correspond to claim 6, claims 7 and 21 correspond to claim 7, claims 8 and 22 correspond to claim 8, claims 9-14 correspond to claims 9-14 of U.S. Application 10/791,241. Although the conflicting claims are not identical, they are not patentably distinct from each other because the scope of the claims 1-22 of this application covers the scope of claims 1-14 of U.S. Application 10/791,241 wherein the claims of the other application has a broader scope than that of this application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by De et al (6100751).

Regarding claim1, De et al disclose [see Fig. 4] an apparatus (see **Note** below) comprising: a device under test (transistor 54, 56, 60 or 62) adapted to received a body bias voltage [known in the prior art as Vbb see col. 3, line 61 and col. 5, lines 6-8 and lines 13-16]; a voltage supply (voltage source 68 or 80) for providing said body bias voltage to said device under test (54, 56, 60 or 62); and a wiring board (circuit board 50) for coupling said device under test (54, 56, 60 or 62) and said voltage supply (68 or 80) wherein said device under test (54, 56, 60 or 62) is subject to a test temperature that is regulated according to said body bias voltage (Vbb).

[Note: The recitation "*for burn-in testing*" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).]

Regarding claim 2, De et al disclose said body bias voltage (Vbb) is selected to achieve a desired junction temperature at said devices under test (54 and 56 or 60 and 62).

Regarding claim 3, De et al disclose a test controller (voltage control circuitry 72) coupled to said devices under test (54 and 56 or 60 and 62) via said wiring board (50).

Regarding claim 4, De et al disclose a voltage supply (shown as VCC) for providing an operating voltage to said devices under test (54 and 56 or 60 and 62).

Regarding claim 5, De et al disclose said devices under test (60 and 62) comprise positive-channel metal-oxide semiconductor (PMOS) devices [see col. 5, line 1].

Regarding claim 6. De et al disclose said body bias voltage (Vbb) is in the range of approximately zero to five volts [see col. 4, lines 19-21].

Regarding claim 7, De et al disclose said devices under test (54 and 56) comprise negative-channel metal-oxide semiconductor (NMOS) devices [see col. 4, line 67-col. 5, line 1].

Regarding claim 8, De et al disclose said body bias voltage (Vbb) is in the range of approximately zero to minus ten volts [see col. 5, lines 24-27 and col. 7, lines 5-6].

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 9-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over De et al (6100751) in view of Hashinaga et al (5406212).

Regarding claim 9, De et al disclose [see Fig. 4] a method of burn-in testing of a device under test (transistor 54, 56, 60, or 62), said method comprising applying an operating voltage [via VCC] to said device under test (54, 56, 60 or 62); and applying a body bias voltage (Vbb) [via voltage source 68 or 80) to said device under test (54, 56, 60 or 62), wherein said body bias voltage (Vbb) is selected to achieve a particular test temperature measured at said device under test. However, De et al do not disclose measuring temperature at said device under test as claimed. Hashinaga et al disclose a method of burn-in testing of a device under test (semiconductor device 33) comprising applying voltage [via power supply means 42] to the device under test (33) and measuring [via temperature detecting unit or sensor 38] temperature at said device under test (33). Further, Hashinaga et al teach that the addition of measuring temperature using sensor 38 is advantageous because it detects electric characteristics of the semiconductor chips so that junction temperatures could be measure on the chips. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of De et al by adding temperature sensor to measure temperature of the device under test as taught by Hashinaga et al in order to detect electric characteristics so that junction temperatures could be measure on the semiconductor chips, which is the device under test.

Regarding claim 10, De et al disclose adjusting said body bias voltage (Vbb) to adjust temperature at said devices under test (54 and 56 or 60 and 62).

Regarding claim 11, De et al disclose said devices under test (60 and 62) comprise positive-channel metal-oxide semiconductor (PMOS) devices [see col. 5, line 1].

Regarding claim 12. De et al disclose said body bias voltage (Vbb) is in the range of approximately zero to five volts [see col. 4, lines 19-21].

Regarding claim 13, De et al disclose said devices under test (54 and 56) comprise negative-channel metal-oxide semiconductor (NMOS) devices [see col. 4, line 67-col. 5, line 1].

Regarding claim 14, De et al disclose said body bias voltage (Vbb) is in the range of approximately zero to minus ten volts [see col. 5, lines 24-27 and col. 7, lines 5-6].

Regarding claim15, De et al disclose [see Fig. 4] an apparatus (see **Note** below) comprising: a plurality of devices under test (transistors 54 and 56 or 60 and 62), each device under test (54, 56, 60 and 62) adapted to receive a body bias voltage [known in the prior art as Vbb see col. 3, line 61 and col. 5, lines 6-8 and lines 13-16]; a voltage supply (voltage source 68 or 80) for providing said body bias voltage to said devices under test (54, 56, 60 and 62); and a wiring board (circuit board 50) comprising circuitry (conductors 78 and 84) that individually couples each said devices under test (54, 56, 60 and 62) to said voltage supply (68 or 80) such that each device under test (54, 56, 60 and 62) can receive a different body bias voltage (Vbb). However, they do not disclose temperature at each device under test is monitored. Hashinaga et al disclose a method of burn-in testing of a device under test (semiconductor device 33) comprising applying voltage [via power supply means 42] to the device under test (33) and monitoring [via temperature detecting unit or sensor 38] the temperature of said device under test (33). Further, Hashinaga et al teach that the addition of monitoring temperature using sensor 38 is advantageous because it detects electric characteristics of the semiconductor chips so that junction temperatures could be measure on the chips. It would have been obvious to

a person having ordinary skill in the art at the time the invention was made to modify the apparatus of De et al by adding temperature sensor to monitor temperature of the device under test as taught by Hashinaga et al in order to detect electric characteristics so that junction temperatures could be measure on the semiconductor chips, which is the device under test.

[Note: The recitation "*for burn-in testing*" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).]

Regarding claim 16, De et al disclose said body bias voltage (Vbb) is selected to achieve a desired junction temperature at said devices under test (54 and 56 or 60 and 62).

Regarding claim 17, De et al disclose a test controller (voltage control circuitry 72) coupled to said devices under test (54 and 56 or 60 and 62) via said wiring board (50).

Regarding claim 18, De et al disclose a voltage supply (shown as VCC) for providing an operating voltage to said devices under test (54 and 56 or 60 and 62).

Regarding claim 19, De et al disclose said devices under test (60 and 62) comprise positive-channel metal-oxide semiconductor (PMOS) devices [see col. 5, line 1].

Regarding claim 20, De et al disclose said body bias voltage (Vbb) is in the range of approximately zero to five volts [see col. 4, lines 19-21].

Regarding claim 21, De et al disclose said devices under test (54 and 56) comprise negative-channel metal-oxide semiconductor (NMOS) devices [see col. 4, line 67-col. 5, line 1].

Regarding claim 22, De et al disclose said body bias voltage (Vbb) is in the range of approximately zero to minus ten volts [see col. 5, lines 24-27 and col. 7, lines 5-6].

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Shimizu et al (5119337), Cho (5844429), McClure (6037792 & 6310485), Forbes et al (6104061), Matsou et al (6114866), Leung, Jr. (6157201), Chen (6137301 & 6262588), and Soumyanath et al (6218892) disclose a method and apparatus for a burn-in board testing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on (517) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Examiner
Art Unit 2829

JMH
August 28, 2004